Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Previously presented) A method for operating a synchronous digital system having clock means for synchronously controlling operation of system logic with toleration of error in logic operation, the method including the steps of:

providing a logic operation input;

increasing clock frequency of the digital system while monitoring the system logic for errors in logic operation output to report a fault;

upon detecting said logic operation fault, slowing the clock frequency associated with the fault to a clock frequency at which no fault is detected; and

employing as logic operation output in place of the current logic operation output a result which is known to be correct for said logic operation input.

3. (Previously presented) The method according to claim 2 wherein the digital system comprises at least two structurally identical pipelines, each said pipeline having registers which accept logic operation successively and which yield logic operation successively, including the step of causing the clock frequency for each said pipeline to operate with a different phase but with identical frequency.

4. (Previously presented) The method according to claim 2 wherein the digital system comprises a pipeline having an input register and an output register for each combinational logic component, wherein the logic operation input step comprises supplying the logic operation input to said combinational logic from the input register in response to a first clock; thereafter

comparing for identity, in response to a second clock, input values and output values of the output register receiving output from the combinational logic, said second clock being identical to but out of phase with said first clock; and

upon detecting lack of identity, delaying operation of said first clock until said identity obtains.

5. (Previously presented) A synchronous digital system having logic operation input and logic operation output comprising:

clock means for synchronously controlling operation of system logic with toleration of error in logic operation, the clock means including a first clock and at least a second clock, said second clock being identical to and out of phase with said first clock;

a comparator associated with said second clock for monitoring the system logic for errors in logic operation output to report a fault; and

clock control logic for increasing clock frequency of the digital system upon detecting said logic operation fault, and upon detecting the fault, being operative to add a delay to the first clock and thereby to the second clock such that a known good output is obtained from a delayed clock and the clock is operative at a frequency at which no fault is detected.

6. (Previously presented) A method for operating a synchronous digital system having clock means for synchronously controlling operation of system logic with avoidance of timing error, the method including the steps of:

providing a logic operation input to tracking logic, said tracking logic representing a worst case delay path for said system logic;

increasing clock frequency of the digital system while monitoring the tracking logic for errors in logic operation output to report a fault;

upon detecting said tracking logic operation fault, slowing the clock frequency associated with the fault to a clock frequency at which no fault is detected.

7. (Previously presented) The method according to claim 6, further including the step of thereafter increasing said clock frequency until a fault reoccurs.

8. (Previously presented) The method according to claim 7, wherein the tracking logic includes a operational safety margin to guarantee that a fault occurs in the tracking logic before a fault can occur in the system logic.

9. (Previously presented) The method according to claim 6, wherein input for said tracking logic is a sequence of digital values including alternating logic one and logic zero.

10. (Previously presented) The method according to claim 9, wherein input for said tracking logic is a digital bit stream of alternating logic ones and logic zeroes.

11. (Previously presented) The method according to claim 6, wherein logic transition timing alone determines transition to a too fast state and transition to a too slow state.

12-18. (Canceled)